QDD-DCQG-ZR+

400G ZR+ QSFP-DD Coherent Optical Module

Features

- Operating rate up to 478.75 Gbps
- PM-QPSK (200G) and PM-16QAM (200G / 400G) modulation formats
- 400GE, 200GE and OTU4 / OTUCn services
- Hot-pluggable QSFP-DD form factor
- 8 × CEI-56G-VSR electrical interfaces
- QSFP-DD-Hardware-rev6p3 compliant
- QSFP-DD-CMIS-rev5p2 compliant
- Lock registers
- Maximum power consumption: 24 W

1 Applications

The module is designed for ZR 400G DCI / PTN applications and ZR+200G metro long-haul OTN applications. It provides high-speed data channels, IIC interface module control and state alarm reporting with 3.3 V power supplied.

2 General

The QSFP-DD coherent optical module uses a 76-pin connector as an electrical interface to connect the system board. The module comprises TX unit, RX unit and control units. All control interface pins work properly with the help of the internal MCU which itself can also be used for modulator control, software management, alarm performance reporting and other functions.

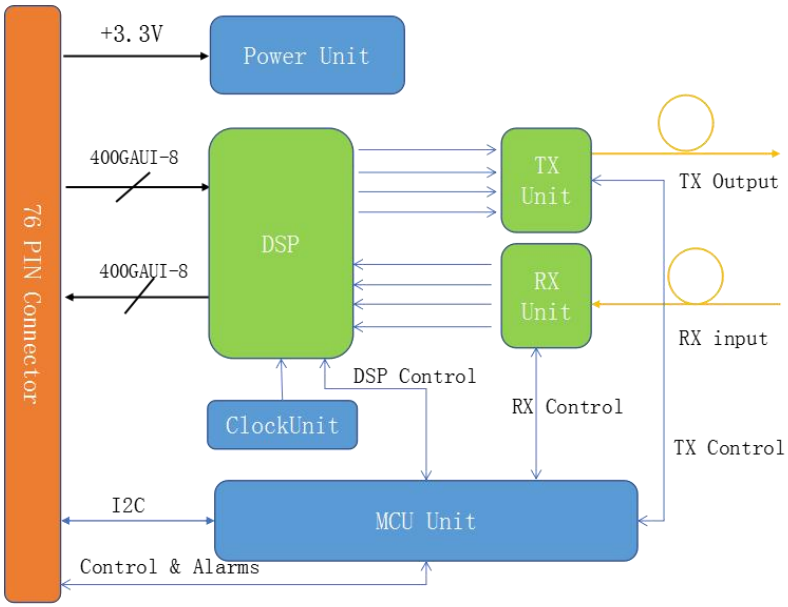

Figure 1 Module Block Diagram

3 Module Characteristics

3.1 200G Optical Port

Table 1 200G Optical Port Performance Specifications

Parameter	Value
Network lane, modulation format	PM-QPSK
Optical channels	80
Grid spacing	75 GHz
Frequency range	190.7 to 196.65 THz
Wavelength stability	±1.5 GHz
Tx output power, default	-0.5 dBm

Parameter	Value
Max. Tx output power	-0.5 dBm
Min. Tx output power	-6 dBm
Tx output power accuracy	±1.5 dB
Output power during tuning	< -35 dBm
CD tolerance	±40 000 ps/nm
DGD tolerance	33 ps
Input power range	0 to -18 dBm
OSNR tolerance (BOL)	15 dB (Rx optical power: -8 to -10 dBm)
Power consumption	Typical: 22 W Maximum: 24 W

Parameter	Value
Network lane, modulation format	PM-16QAM
Optical channels	96
Grid spacing	50 GHz
Frequency range	191.3 to 196.05 THz
Wavelength stability	±1.5 GHz
Tx output power, default	-0.5 dBm
Max. Tx output power	-0.5 dBm
Min. Tx output power	-6 dBm
Tx output power accuracy	±1.5 dBm
Output power during tuning	< -35 dBm
CD tolerance	±10 000 ps/nm
DGD tolerance	22 ps
Input power range	0 to -18 dBm
OSNR tolerance (BOL)	19.5 dB (Rx optical power: -8 to -10 dBm)
Power consumption	Typical: 18 W Maximum: 20 W

3.2 400G Optical Port

Table 2 400G Optical Port Performance Specifications

Parameter	Value
Network lane, modulation format	PM-16QAM（ZR+）
Optical channels	80
Grid spacing	75 GHz
Frequency range	190.7 to 196.65 THz
Wavelength stability	±1.5 GHz
Tx output power, default	-0.5 dBm
Max. Tx output power	-0.5 dBm
Min. Tx output power	-6 dBm
Tx output power accuracy	±1.5 dBm
Output power during tuning	< -35 dBm
CD tolerance	±9 000 ps/nm
DGD tolerance	22 ps
Input power range	0 to -10 dBm
OSNR tolerance (BOL)	24 dB (Rx optical power: -8 to -10 dBm)
Power consumption	Typical: 22 W Maximum: 24 W

4.3 Electrical Characteristics

4.3.1 Power Supply Requirements

The QSFP-DD coherent optical module has six designated pins on the 76-pin connector for its own power feed. The host board supplies a stable power to the module which in turn limits the inrush charging current of the hot-swappable devices. Power feed to all internal devices in the optical module is converted from the host board through the connector. Table 3 describes the power supply requirements. All voltages are tested at the connector interface.

Table 2 QSFP-DD Coherent Optical Module Power Supply Requirements

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccTx1, VccRx, VccRx1, Vcc1 & Vcc2 including ripple, droop and noise below 100kHz[1]		3.135	3.3	3.465	V
Host RMS noise output 40 Hz-10 MHz				25	mV
Module RMS noise output 10 Hz - 10 MHz				30	mV
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak)	$PSNR_{mod}$			66	mV
Module inrush - instantaneous peak duration[2]	T_ip			50	µs
Module inrush - initialization time[4]	T_init			500	ms
Low Power Mode					
Power Consumption	P_lp			1.5	W
Instantaneous peak current at hot plug	Icc_ip_lp	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_lp	-	-	495	mA
Steady state current	Icc_lp		See Note 3		mA
High Power Mode Power Class 1 module					
Power Consumption	P_1			1.5	W
Instantaneous peak current	Icc_ip_1	-	-	600	mA
Sustained peak current	Icc_sp_1	-	-	495	mA
Steady state current	Icc_1		See Note 3		mA
High Power Mode Power Class 2 module					
Power Consumption	P_2			3.5	W
Instantaneous peak current	Icc_ip_2	-	-	1400	mA
Sustained peak current	Icc_sp_2	-	-	1155	mA
Steady state current	Icc_2		See Note 3		mA
High Power Mode Power Class 3 module					
Power Consumption	P_3			7	W
Instantaneous peak current	Icc_ip_3	-	-	2800	mA
Sustained peak current	Icc_sp_3	-	-	2310	mA
Steady state current	Icc_3		See Note 3		mA
High Power Mode Power Class 4 module					
Power Consumption	P_4			8	W
Instantaneous peak current	Icc_ip_4	-	-	3200	mA
Sustained peak current	Icc_sp_4	-	-	2640	mA
Steady state current	Icc_4		See Note 3		mA
High Power Mode Power Class 5 module					
Power Consumption	P_5			10	W
Instantaneous peak current	Icc_ip_5	-	-	4000	mA
Sustained peak current	Icc_sp_5	-	-	3300	mA
Steady state current	Icc_5		See Note 3		mA
High Power Mode Power Class 6 module					
Power Consumption	P_6			12	W
Instantaneous peak current	Icc_ip_6	-	-	4800	mA
Sustained peak current	Icc_sp_6	-	-	3960	mA
Steady state current	Icc_6		See Note 3		mA
High Power Mode Power Class 7 module					
Power Consumption	P_7			14	W
Instantaneous peak current	Icc_ip_7	-	-	5600	mA
Sustained peak current	Icc_sp_7	-	-	4620	mA
Steady state current	Icc_7		See Note 3		mA
High Power Mode Power Class 8 module					
Power Consumption	P_8[4]			>14	W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8	-	-	6	A

Note 1: Measured at VccTx, VccTx1, VccRx, VccRx1, Vcc1 and Vcc2
Note 2: T_ip and T_init are test conditions for measuring inrush current and not characteristics of the module
Note 3: The module must stay within its declared power class.
Note 4: User must read management register for maximum power consumption

4.3.2 High-Speed Electrical Interface Specifications

The QSFP-DD coherent optical module provides multiple electrical interfaces. For details, see Table 4.

Table 4 QSFP-DD Coherent Optical Module

Client Type	Interface Type	Electrical Standards
100GE	CAUI-4	IEEE 802.3bm CAUI-4 Chip-to-Module
100GE	100GAUI-2	IEEE 802.3bm GAUI-8 Chip-to-Module
200GE	200GAUI-8	OIF CEI-28G VSR
200GE	200GAUI-4	IEEE 802.3bm GAUI-8 Chip-to-Module
400GE	400GAUI-8	
OTU4	OTL4.4	OIF CEI-28G VSR
OTU4	OTL4.2	OIF CEI-56G VSR PAM-4
OTUC1 / OTUC2	FOIC1.4 (FlexO-SR)	OIF CEI-28G VSR
OTUC1 / OTUC2 / OTUC3 / OTUC4	FOIC1.2 (FlexO-SR)	OIF CEI-56G VSR PAM-4
OTUC4	FOIC4.8 (FlexO-SR)	OIF CEI-56G VSR PAM-4

4.3.2.1 REFCLK (Reference Clock)

The QSFP-DD coherent optical module does not require the host board to provide a reference clock (REFCLK).

4.3.2.2 TXMCLK (Transmitter Monitor Clock)

The Tx side of the QSFP-DD coherent optical module does not provide a monitor clock (TXMCLK) for monitoring Tx optical signals.

4.3.3 Control Pins (non-IIC) Functional Description

4.3.3.1 ModSelL (Module Selection)

Module selection (ModSelL) is an input pin which is pulled up to Vcc in the module. When ModSelL is driven low by the host, the module responds to serial communication commands from the IIC bus. The ModSelL allows the use of multiple QSFP-DD modules at one IIC interface bus. When ModSelL is driven high by the host, the module does not respond to any command from the IIC interface. To avoid conflicts, after deselecting all QSFP-DD modules, the host should not attempt to communicate through the IIC interface during the ModSelL failure time. Similarly, the host should wait at least one ModSelL effective cycle before communicating with the newly selected QSFP-DD module. For details about ModSelL Setup Time (tSU.ModSelL) and ModSelL Hold Time (tHD.ModSelL), see Table 8.

4.3.3.2 MOD_LOPWR (Module Low Power)

MOD_LOPWR is a signal input pin from the host and works in the logic high state. When MOD_LOPWR is logic high, the optical module works at low power consumption and remains in this mode. When MOD_LOPWR is pulled low, the optical module is initialized to a high power consumption mode, that is, the normal operation mode. In low power consumption mode, the optical module communicates through the MDIO management interface, and its maximum power consumption does not exceed 2 W. Refer to Table 8 for the timing diagram of MOD_LOPWR. For values of "t_MOD_LOPWR_on" and "t_ MOD_LOPWR_off", see Figure 4.

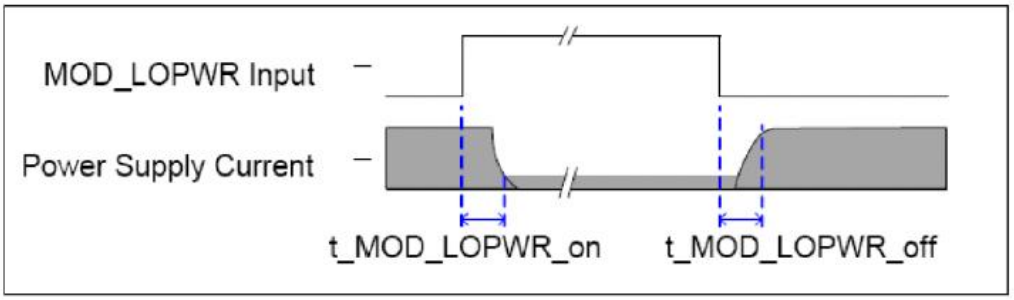

Figure 4 Timing Diagram for MOD_LOPWR

4.3.3.3 ResetL (Module Reset)

ResetL is a signal input pin which is pulled up to Vcc in the module. The QSFP-DD module is completely reset when ResetL is driven by a low level signal with a pulse length longer than the minimum pulse length (t_Reset_init). After reset, all user settings of the module are restored to their default states.

4.3.4 Alarm Pins (non-MDIO) Functional Description

4.3.4.1 RX_LOS (Receiver Loss of Signal)

RX_LOS is a signal output pin which transmits signals to the host board and works at the logic high state. When RX_LOS is logic high, the optical power received by the optical module is too low. Figure 5 shows the timing diagram for RX_LOS.

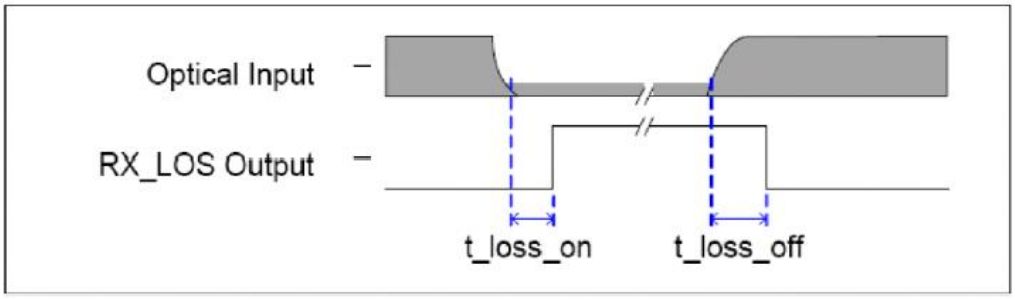

Figure 5 Timing Diagram for RX_LOS

4.3.4.2 MOD_ABS (Module Absent)

MOD_ABS is a signal output pin which transmits signals from the inside of the module to the host board. This pin is pulled up on the host board but pulled down to the ground inside the

module. When the optical module is inserted into the host board, MOD_ABS is logic low, meaning that the module is present. When no optical module is on the host board, MOD_ABS is logic high, meaning that the module is absent.

4.3.5 Control and Alarm Descriptions

4.3.5.1 Timing Parameters for Control and Alarm Signals

Table 6 Signal Timing Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter Disabled (TX_DIS high)	t_off			100	μs	Application specific. Defined by module vendor.
Transmitter Enabled (TX_DIS low)	t_on			25	s	Application specific. Defined by module vendor.
MOD_LOPWR assert	t_MOD_LOPWR _assert			9.5	s	Application specific. Defined by module vendor.
MOD_LOPWR deassert	t_MOD_LOPWR _deassert	0.1		10	s	Application specific. Defined by module vendor.
Receiver Loss of Signal Assert Time	t_loss_on	0.5		400	μs	Application specific. Defined by module vendor.
Receiver Loss of Signal De-assert Time	t_loss_off	0.5		400	μs	Application specific. Defined by module vendor.
Management Interface Clock Period	tprd	250			ns	MDC is 4 MHz rate
Host MDIO setup time	tsetup	4			ns	
Host MDIO hold time	thold	3.2			ns	
Module MDIO delay time	tdelay	0		175	ns	
Initialization time from Reset	t_initialize	19		120	s	

4.3.5.2 Control and Alarm Pins: 3.3V LVCMOS Electrical Characteristics

The hardware control and alarm pins specified as 3.3V LVCMOS functionality described above shall meet the electrical characteristics described in Table 7. Their reference input and output termination modes are shown in Figure 6.

Table 7 3.3V LVCMOS Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	3.2	3.3	3.4	V
Input high voltage	VIH	2		VCC+0.3	V
Input low voltage	VIL	-0.3		0.8	V
Input leakage current	IIN	-10		10	μA
Output high voltage (I_{OH} = -100 μA)	VOH	VCC-0.2			V
Output low voltage (I_{OL} = 100 μA)	VOL			0.2	V

Figure 2-6: Reference +3.3V LVCMOS Output Termination

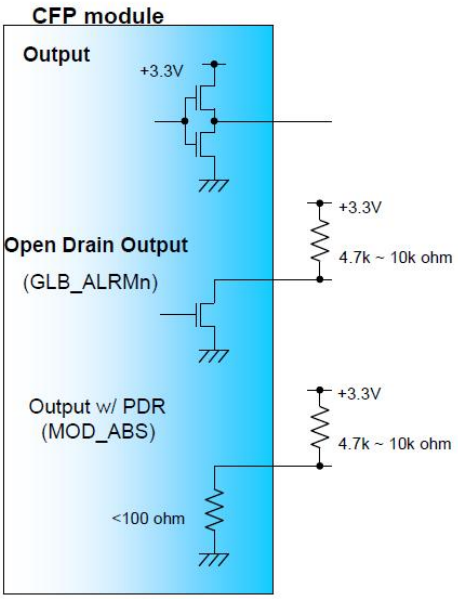

Figure 2-7: Reference +3.3V LVCMOS Input Termination

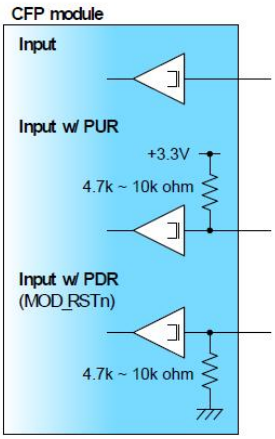

Figure 6 Reference 3.3V LVCMOS Input / Output Termination

4.3.6 Module Management Interface (IIC) Description

4.3.6.1 Management Data Input / Output Interface (IIC)

The QSFP-DD module uses IIC to communicate with related cores on host ASICs. As a hot-swappable interface, the IIC interface supports bus topologies.

4.3.6.2 Management Data Clock Pins (SCL)

The host defines a default clock rate of up to 400 KHz for the IIC, optionally supporting up to 1 MHz. Figure 7 shows the timing diagram for SCL and SDA pins and Table 8 describes their specific timing parameters. This section strictly conforms to the QSFP SFF-8636 specifications.

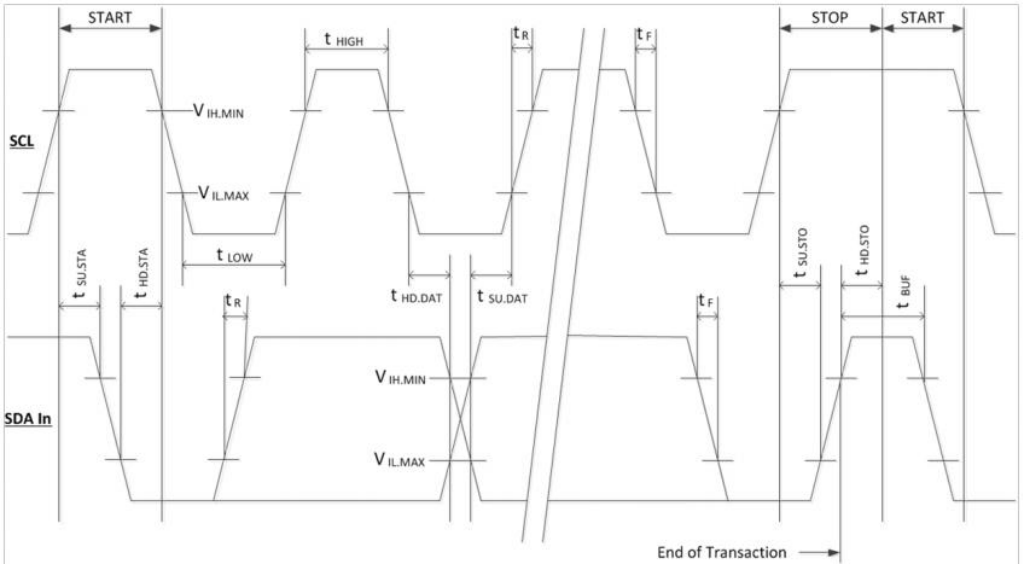

Figure 7 Timing Diagram for the SCL & SDA Pins

Table 8 IIC Interface Timing Parameters

		Fast Mode (400 kHz)		Fast Mode Plus (1 MHz)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3		0.50		μs	
Clock Pulse Width High	tHIGH	0.6		0.26		μs	
Time bus free before new transmission can start	tBUF	20		1		μs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		μs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		μs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		μs	
Data In Setup Time	tSU.DAT	0.1		0.1		μs	
Input Rise Time	tR		300		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		300		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.26		μs	
STOP Hold Time	tHD.STO	0.6		0.26		μs	
Aborted sequence - bus release	Deselect_Abort		2		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time[1]	tSU.ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated serial bus sequence.
ModSelL Hold Time[1]	tHD.ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module select status.
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500		500	us	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write to non-volatile registers	tWR		80		80	ms	Complete Write of up to 8 Bytes
Accept a single or sequential write to volatile memory.	tNACK		80		80	ms	Time required for the module to accept a single or sequential write to volatile memory.
Endurance (Write Cycles)		50K			50k	cycles	Module Case Temperature = 70° C
Note 1: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.							

4.3.6.3 IIC Physical Interface Address Pin (ModSelL)

The serial port address of the IIC interface is 1010000X (A0h). To access to multiple QSFP-DD modules on one IIC serial bus, each QSFP-DD's 76-pin connector provides a module selection pin (ModSelL). ModSelL is pulled high by default, meaning the corresponding module is not selected. If it is pulled low by the host, this module is selected and can communicate with the host through the IIC interface.

4.3.6.4 IIC Interface Pins: Vcc-based LVCMOS Electrical Characteristics

The IIC pins working in Vcc-based LVCMOS mode described above shall meet the electrical characteristics described in Table 9. Their reference input and output termination modes are shown in Figure 9.

Table 9 Vcc-based LVCMOS Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3 mA for fast mode, 20 mA for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3.0 k Ohms Pullup resistor, max. For 1000 kHz clock rate
			200	pF	For 400 kHz clock rate use 1.6 k Ohms pullup resistor, max.
LPMode, ResetL, ModSelL and Epps	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
LPMode, ResetL and ModSelL	|Iin|		360	μA	0V<Vin<Vcc

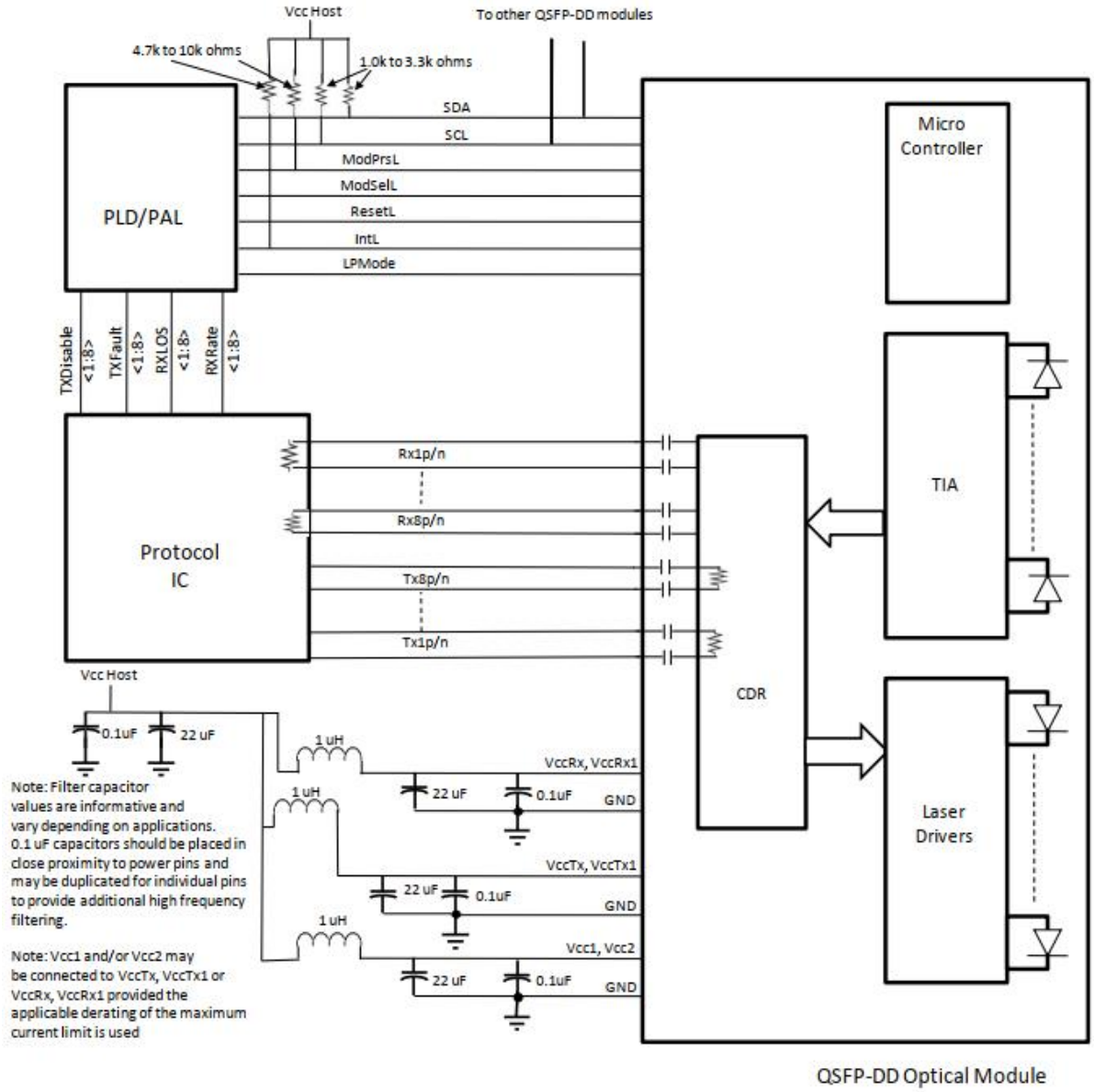

Figure 9 IIC Interface Reference Termination Mode

4 Operating Environment

Table 10 Operating Environment

Parameter	Min.	Max.	Unit	Notes
Storage temperature	-40	85	ºC	
Operating case temperature	0	70	ºC	
Relative humidity, operating (non-condensing)	5	85	%	

Relative humidity, operating (short term < 96 hrs, non-condensing)	5	95	%	
ESD sensitivity (HBM)		High-speed pins: 500 Other pins: 2000	V	

5 Pin Assignment and Description

Electrical connections of 76 pins include eight pairs of TX differential signals (input TXIs of the module, connecting to signal outputs of the card), eight pairs of RX differential signals (output RXOs of the module, connecting to signal inputs of the card), control pins, alarm pins, IIC communication related pins, GND pins, +3.3V power supply pins and some reserved pins.

Table 11 Pin Assignment

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.

6 Mechanical Dimensions

Figure 10 shows mechanical dimensions of the QSFP-DD coherent optical module.

Max. dimensions (L × W × H): 93.3 mm × 18.35 mm × 8.5 mm.

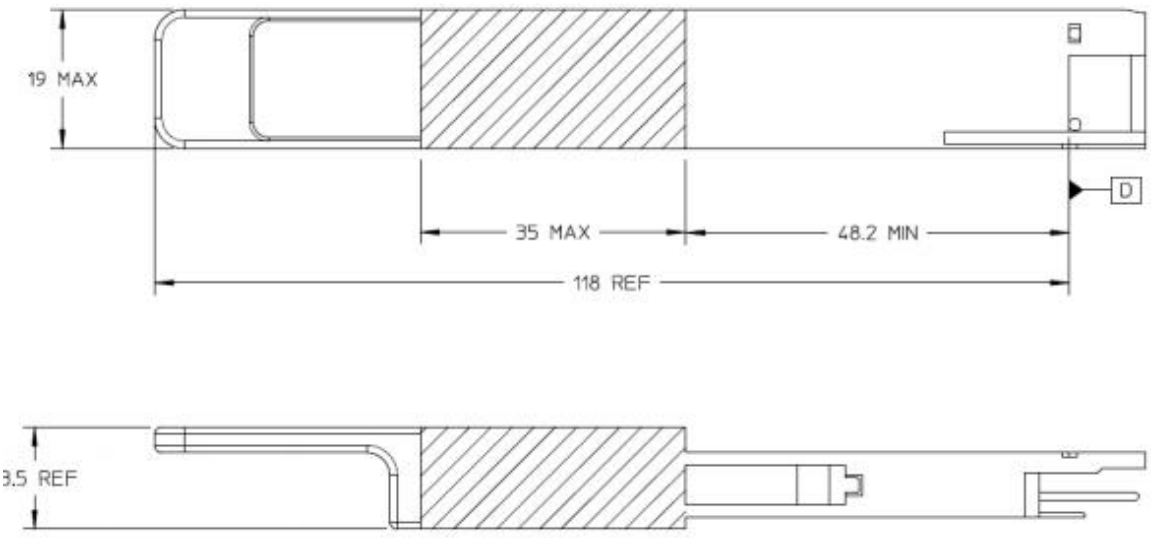

Figure 10 Mechanical Dimensions of the QSFP-DD Optical Module

7.Ordering information

Part Number	Product Description
QDD-DCQG-ZR+	400G QSFP-DD Coherent Optical Module

8.For More Information

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