QFP-DWxxHG-80DC

100Gbps QSFP28 DWDM Transceiver, 80km Reach

Features

- Supports 100Gbps
- Available in all C-Band Wavelengths
- 100GHz DWDM ITU Grid
- Single 3.3V Power Supply
- Power Dissipation < 5.5W
- 80km reach over SMF with EDFA&DCM (dispersion compensation modules)
- QSFP28 MSA Compliant
- SFF-8636 Rev 2.10a Compliant
- 4x25G Electrical Interface
- LC Duplex Connector
- I^2C Interface with Integrated Digital Diagnostic Monitoring
- Safety Certification: TUV/UL/FDA
- RoHS Compliant
- Commercial Case Temperature Range of 0°C to 70°C

Applications

- 100G Amplified DWDM Networks
- Data Center Interconnects

Product Description

The QFP-DWxxHG-80DC series single mode transceiver module is designed for use in duplex optical data communications. This module is designed for single mode optical fiber and operates at a data rate of 100Gbps at the nominal DWDM wavelength from 1528.77nm to 1565.50nm as specified by the ITU-T. This module can convert 4 channels of 25Gbps (NRZ) electrical input data to 1 channel of 100Gbps (PAM4) optical signal, and also can convert 1 channel of 100Gbps (PAM4) optical signal

to 4 channels of 25Gbps (NRZ) electrical output data. The electrical interface of the module is compliant with the OIF CEI-28G-VSR and QSFP28 MSA. It is designed to deploy in the DWDM networking equipment in metropolitan access and core networks.

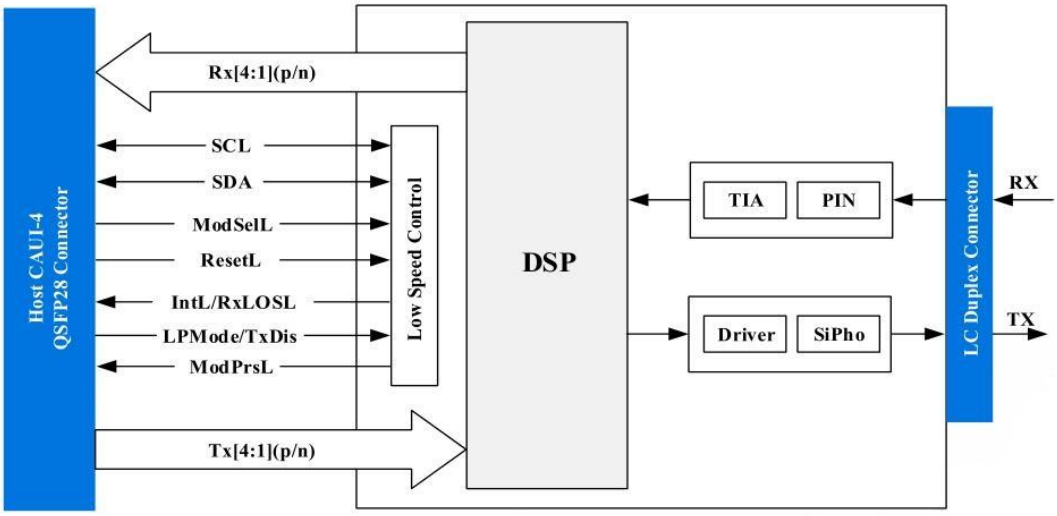

Figure 1: Transceiver Block Diagram

Only one channel i (i=1, 2, 3, 4) shown for simplicity

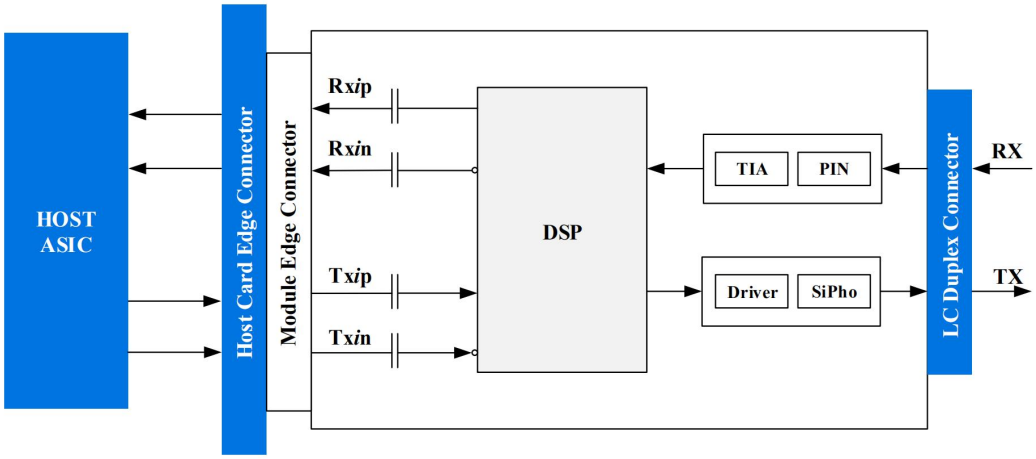

Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the transmitter path of the transceiver contains a 4x25Gbps CAUI-4 electrical input, integrated electrical multiplexer, SiPho driver, diagnostic monitor, control and bias for the MZ modulator and single mode laser source. The integrated electrical multiplexer converts 4 channels of 25Gbps (NRZ) electrical input data to 1 channel of 100Gbps (PAM4) optical signal.

Receiver

As shown in Figure 1, the receiver path of the transceiver contains a PIN photodiode, trans-impedance amplifier (TIA), integrated de-multiplexer and 4x25Gbps CAUI-4 compliant electrical output block. The integrated de-multiplexer converts 1 channel of 100Gbps (PAM4) optical signal to 4 channels of 25Gbps (NRZ) electrical output data.

High Speed Electrical Signal Interface

The interface between QSFP28 module and Host ASIC is shown in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to CAUI-4 specification per IEEE 802.3cd.

Control Signal Interface

The module has the following low speed signals for control and status: ModSelL, ResetL, LPMode/TxDis, ModPrsL, IntL/RxLOSL. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are further defined in the Control Interface& Memory Map section.

Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment, and attention should also be taken to restrict exposure to the conditions defined in the absolute maximum ratings.

Optical connectors will be exposed as long as the port plug is not inserted, so always pay attention toprotection. Each module is equipped with a port guard plug to protect the optical ports. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard LC port cleaning methods.

Absolute Maximum Ratings

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min	Typical	Max	Units
Storage Temperature	T_S	-40		+85	℃
Supply Voltage	V_{CC}	-0.5		+3.6	V
Damage Threshold	Rxdmg	5.5			dBm

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	Tc	0		70	degC	2
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Operating Relative Humidity	RH	5		85	%	
Power Dissipation	P_D			5.5	W	
Electrical Signal Rate			25.78125		Gbps	
Optical Signal Rate			53.125		Gbaud	
Power Supply Noise				66	mVpp	3
Receiver Differential Data Output Load			100		Ohm	
Fiber Length (9μm SMF)				80	Km	4

Notes:

1. Power supply specifications, instantaneous, sustained and steady state current are compliant with QSFP28 MSA power classification.
2. The position of case temperature measurement is shown in Figure 9. Continuous operation at the maximum recommended operating case temperature should be avoided in order not to degrade reliability.
3. Power supply noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.
4. 9μm SMF. The maximum link distance is based on an allocation of 1dB of attenuation and 3dB total connection and splice loss. The loss of a single connection shall not exceed 0.5dB.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
High Speed Transmitter (@TP2 Test Point)						
Signaling Speed			53.125		Gbaud	
Center Wavelength Spacing			100		GHz	
			0.8		nm	
Spectral Width (-20dB)	Δλ			0.3	nm	
Modulation Format			PAM4			
Deviation From Central Frequency@EOL		-12.5		12.5	GHz	
Side-Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	3.5			dB	
Transmit OMA	TxOMA	-4.8		4.2	dBm	
Transmit Average	TxAVG	-7		4	dBm	1
Dispersion Tolerance	TD	-40		20	ps/nm	
Optical Return Loss Tolerance				17.1	dB	2
High Speed Receiver (@TP3 Test Point)						
Signaling Speed			53.125		Gbaud	
Center Wavelength	λc	1528		1566	nm	
Damage Threshold	Rxdmg	5.5			dBm	
Average Receive Power	RxAVG	-3		4.5	dBm	4
Receive Power (OMA Outer)	RxOMA			4.7	dBm	
Receiver Sensitivity (OMA Outer)	SenOMA			Max (-4.5, SECQ-5.9)	dBm	3
Receiver Reflectance				-26	dB	
LOS Assert	LOSA	-15			dBm	
LOS De-Assert	LOSD			-12	dBm	
LOS Hysteresis		0.5	-		dB	

Note:

1. Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.
3. Sensitivity is specified at $2.4x10^{-4}$ BER with PRBS31Q

4. Receiver range is specified at BER<2.4x10^{-4} and OSNR is 34dB.

Electrical Characteristics

Parameter	Test Point	Min	Typical	Max	Units	Condition	Notes
Transceiver Power Consumption				5.5	W		
Transceiver Power Supply Current, Total				1757	mA		
Ac Coupling Capacitors (Internal)			0.1		μF		
High Speed Transmitter Input							
Differential pk-pk Input Voltage Tolerence	TP1a	900			mV_{p-p}		
Differential Input Impedance	TP1	90	100	110	Ohm		
Output Rise/Fall Time	TP1a	10			ps	20%~80%	
Eye Width	TP1a	0.46			UI	1E-15	
Eye Height , Differential	TP1a	95			mV	1E-15	
Dc Common Mode Voltage (Vcm)	TP1	-350		2850	mV		1
High Speed Output							
Differential pk-pk Output Voltage	TP4			900	mV_{p-p}		
Differential Output Impedance	TP4	90	100	110	Ohm		
Output Rise/Fall Time	TP4	12			ps	20%~80%	
Eye Width	TP4	0.57			UI	1E-15	
Eye Height Differential	TP4	228			mV	1E-15	
Dc Common Mode Voltage (Vcm)	TP4	-350		2850	mV		1

Notes:
1. Vcm is generated by the host. Specification includes effects of ground offset voltage.

Reference Points

Reference Point	Description
TP0	Host ASIC transmitter output at ASIC package contact.
TP1	Input to module compliance board through mated module compliance board and module connector. Used to test module input.
TP1a	Host ASIC transmitter output through the host board and host card edge connector at the output of the host compliance board. Also used to calibrate module input compliance signals.

TP4	Module output through the compliance board connectors at the output of the module compliance board. Also used to calibrate host input compliance signals.
TP4a	Input to host compliance board. Used to test host input.
TP5	Input to host ASIC
TP5a	Far end module output through a reference channel.
Note: Individual standards may specify unique reference points.	

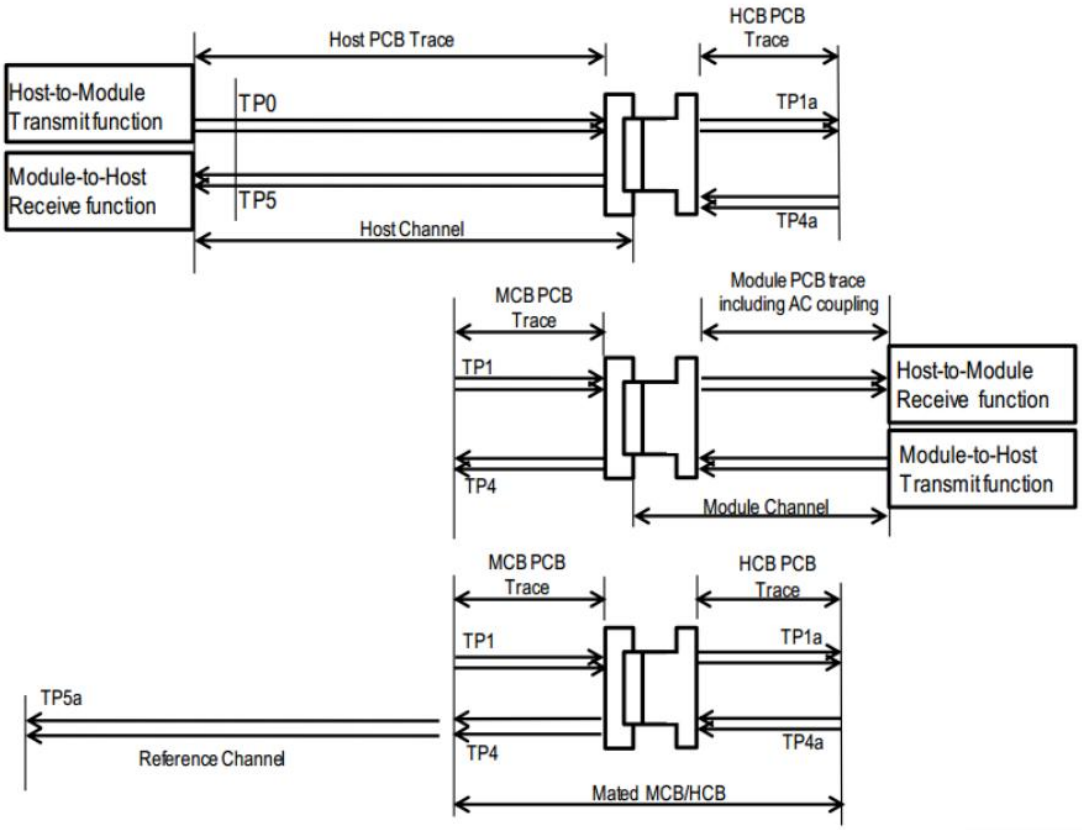

Figure 3: Reference points and compliance boards

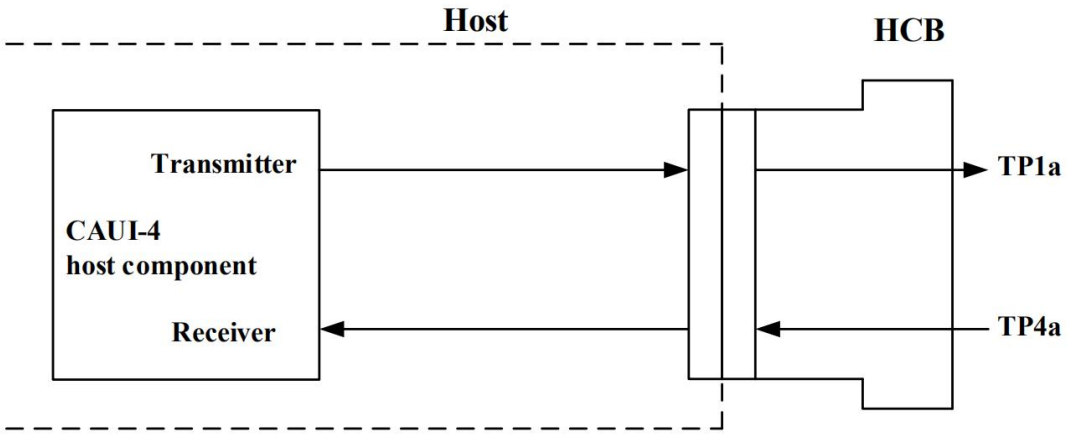

Figure 4: IEEE 802.3 CAUI-4 compliance points TP1a, TP4a

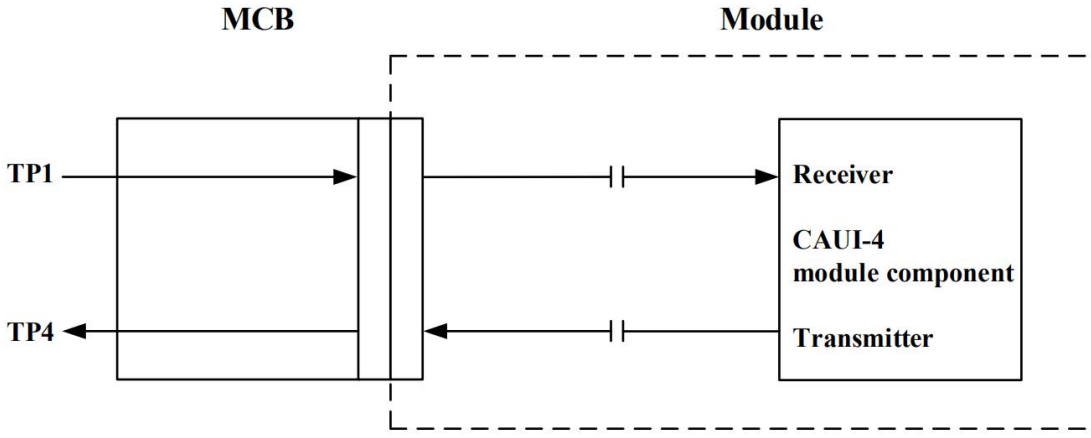

Figure 5: IEEE 802.3 CAUI-4 compliance points TP1, TP4

Pin Assignment

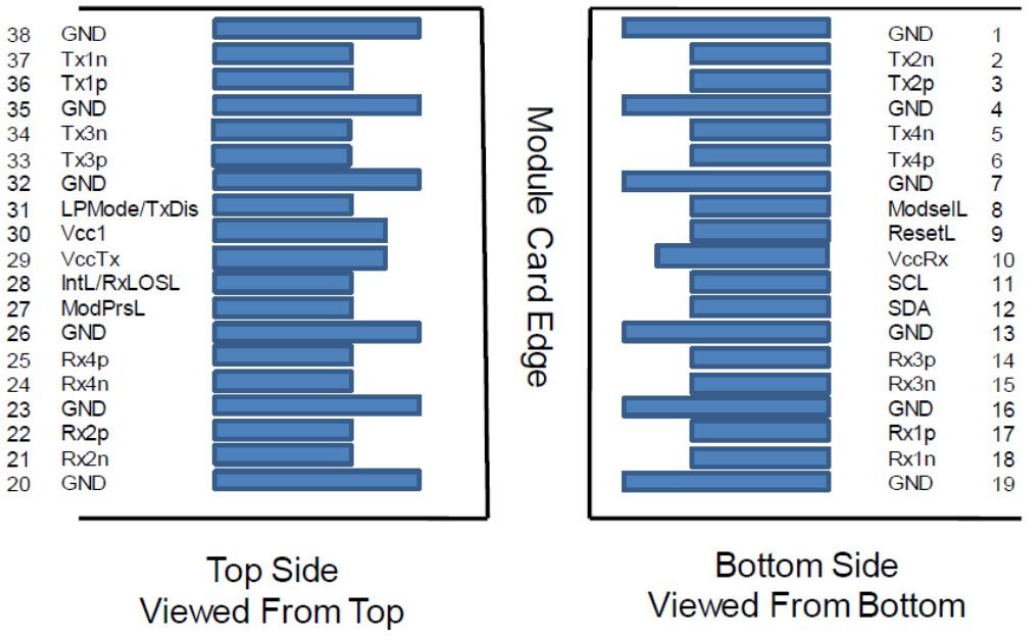

Figure 6: MSA Compliant Connector

Pin Definition

Pin	Logic	Symbol	Description	Plug Sequence	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	

16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/ RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface	3	
29		VccTx	+3.3V Power Supply Transmitter	2	2
30		Vcc1	+3.3V Power Supply	2	2
31	LVTTL-I	LPMode/ TxDis	Low Power Mode. Optionally configurable as TxDis via the	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect them directly to the host board signal-common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and applied concurrently. VccRx, Vcc1 and VccTx are internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1A.

Recommended Power Supply Filter

During power transient events, the host should ensure that any neighboring modules sharing the same supply stay within their specified supply voltage limits. The host should also ensure that the intrinsic noise of the power rail is filtered in order to guarantee the correct operation of the optical modules.

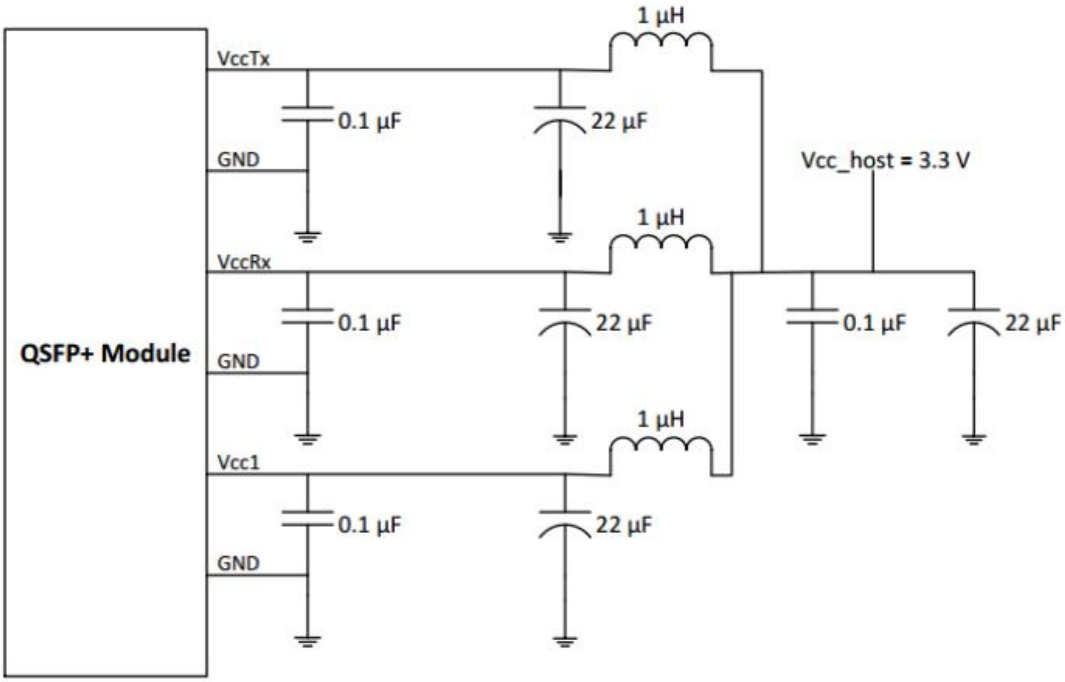

Figure 7: Host Board Power Supply Filter

Control Interface & Memory Map

The control interface combines dedicated signal lines for ModSelL, ResetL, LPMode/TxDis, ModPrsL, IntL/RxLOSL, two-wire serial interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

ModSelL

ModSelL is an input signal. When held low by the host, the module responds to two-wire serial communication commands. When ModSelL is high, the module can't respond to or acknowledge any two-wire interface communication from the host. The ModSelL signal input node is pulled up towards Vcc in the module with a resistor of 10k . In order to avoid conflicts, the host system won't attempt two-wire interface communications within the ModSelL de-assert time after any modules are

deselected. Similarly, the host will wait at least for the period of the ModSelL assert time before communicating with the newly selected module.

ResetL

The ResetL signal is pulled up towards Vcc in the module with a resistor of 10k . A low level on ResetL for longer than 10μs initiates a complete module reset, returning all user module settings to their default state.

LPMode/TxDis

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It is pulled up towards Vcc in the module with a resistor of 10k . At power-up or after ResetL is de-asserted, the LPMode/TxDis behaves as LPMode. LPMode/TxDis can be configured as TxDis using the two-wire interface except during the execution of a reset.

When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (SFF-8636, Address A0h, Byte 93 bits 0,1,2), the host controls how much power a module can consume.

When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters within the times specified in SFF-8636.

Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state with transmitters already enabled, the module will disable all optical transmitters.

Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits.

ModPrsL

ModPrsL is pulled up towards Vcc on the host board and pulled towards ground in the module. ModPrsL is pulled low when inserted and released to high when it is physically absent from the host connector.

IntL/RxLOSL

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It is pulled up towards Vcc on the host board with a resistor of 10k . At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. IntL/RxLOSL can be optionally programmed as RxLOSL using the two-wire interface except during the execution of a reset.

If IntL/RxLOSL is configured as IntL, a low indicates a possible module operational fault or a module condition that sets an unmasked flag as defined in SFF-8636. The source of the IntL “low” can be read, cleared or masked using the two-wire interface. If the interrupt was after a module reset and SFF-8636,

Page 00h, Byte 2, bit 0 (Data_Not_Ready bit) is 0, then the module releases IntL to high after the host has read the Data_Not_Ready bit. For all other interrupt causes, the module releases IntL to high after the host has read the flag associated with the cause of the interrupt.

If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane, a high indicates that there is no loss of received optical power. The module pulls RxLOSL to low if any lane in a multiple lane module has a LOS condition and release RxLOSL to high only if no lane has a LOS condition.

SCL and SDA

The SCL and SDA is a hot plug interface that can support a bus topology. During module insertion or removal, the module will implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Control Interface Electrical Specifications

Parameter	Symbol	Min	Max	Unit
SCL and SDA	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V
SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V
Capacitance on SCL and SDA I/O Contact	Ci		14	pF
Total bus capacitive load for SCL and SDA	Cb		100	pF
			200	pF

LPMode/TxDis, ResetL and ModSelL	VIL	-0.3	0.8	V
	VIH	2	Vcc+0.3	V
	Iin	-365	125	μA
ModPrsL and IntL/RxLOSL	VOL	0	0.4	V
	VOH	Vcc-0.5	Vcc+0.3	V

Note: Positive values indicate current flowing into the module

Memory Map

The memory is structured as a single address, multiple page approach and is compliant with the QSFP28 MSA. The module meets the following requirements:

1. The module initialize in hardware mode when LPMode is de-asserted.

2. The transmitter is disabled when the module is held in reset.

3. Tx Squelch function is implemented as defined by the QSFP28 MSA. When squelched, the transmitter remains on with the modulation turned off.

4. Rx Squelch function is implemented as defined by the QSFP28 MSA. When RxLOSL is asserted, the receiver output is squelched.

From	To	Content	No. of bytes	Type
2-Wire Serial Address 1010000x				
Lower Page 00h				
0	2	ID and Status	3	Read-Only
3	21	Interrupt Flags (Clear on read)	19	Read-Only
22	33	Free Side Device Monitors	12	Read-Only
34	81	Channel Monitors	48	Read-Only
82	85	Reserved	4	Read-Only
86	99	Control	14	Read/Write
100	106	Free Side Interrupt Masks	7	Read/Write
107	110	Free Side Device Properties	4	Read-Only
111	112	Assigned to PCI Express	2	Read/Write
113	116	Free Side Device Properties	4	Read-Only
117	118	Reserved	2	Read/Write
119	122	Optional Password Change	4	Write-Only
123	126	Optional Password Entry	4	Write-Only
127	127	Page Select Byte	1	Read/Write
Upper Page 00h				
128	128	Identifier	1	Read-Only
129	191	Base ID Fields	63	Read-Only
192	223	Extended ID	32	Read-Only
224	255	Vendor Specific ID	32	Read-Only
Page 01h (Optional)				
128	255	Reserved (previously for SFF-8079 support)	128	Read-Only
Page 02h (Optional)				
128	255	User EEPROM Data	128	Read/Write
Page 03h (Optional)				
128	175	Free Side Device Thresholds	48	Read-Only
176	223	Channel Thresholds	48	Read-Only
224	229	Tx EQ, Rx Output and TC Support	6	Read-Only
230	241	Channel Controls	12	Read/Write
242	251	Channel Monitor Masks	10	Read/Write
252	255	Reserved	4	Read/Write
Pages 04h-1Fh (Optional)				
128	255	Vendor Specific	128	Read/Write
Pages 20h-21h (Optional)				
128	255	PAM-4 and WDM Features	128	Read/Write
Pages 22h-7Fh (Optional)				
128	255	Reserved	128	Read/Write
Pages 80h-FFh (Optional)				
128	255	Vendor Specific	128	Read/Write

Figure 8: QSFP28 MIS Module Memory Map

Mechanical Dimensions

The module is designed to meet the package outline defined in the QSFP28 MSA specification. See the package outline for details.

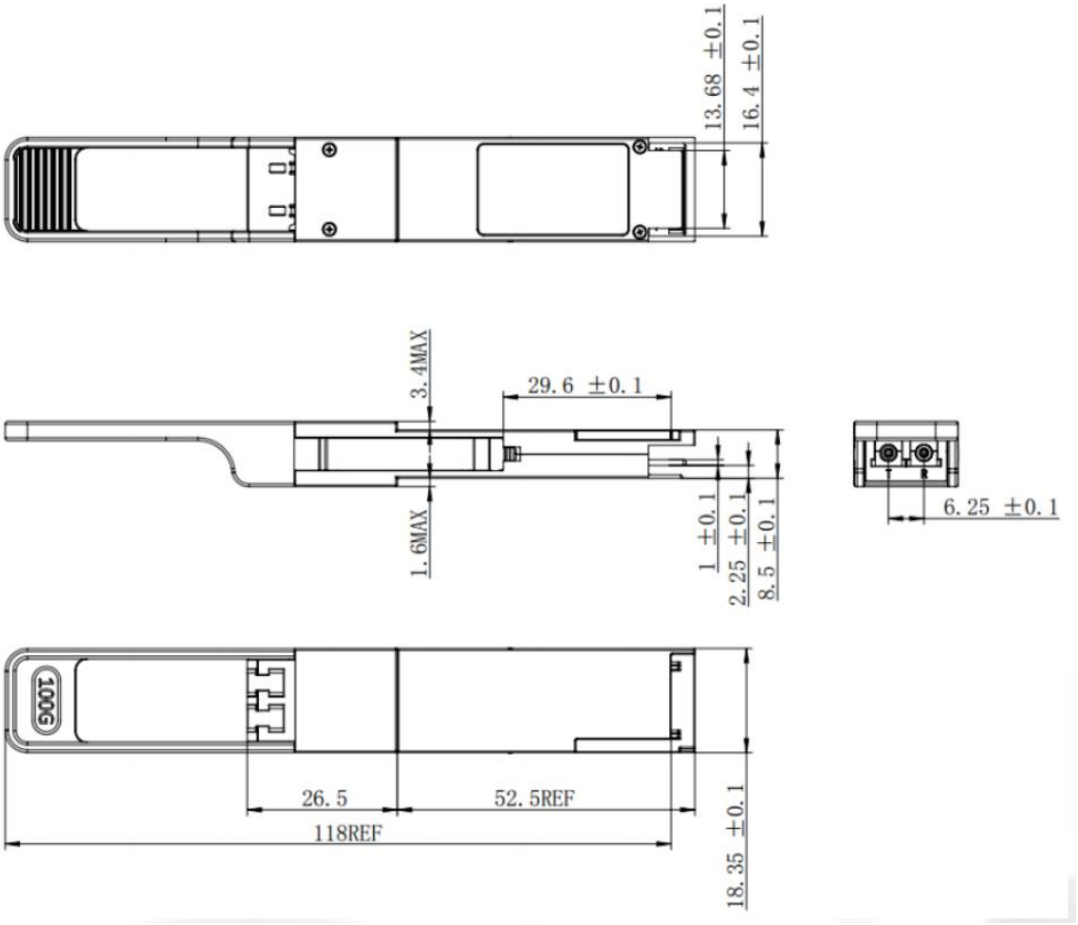

Figure 9: Mechanical Package Outline (Unit: mm)

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

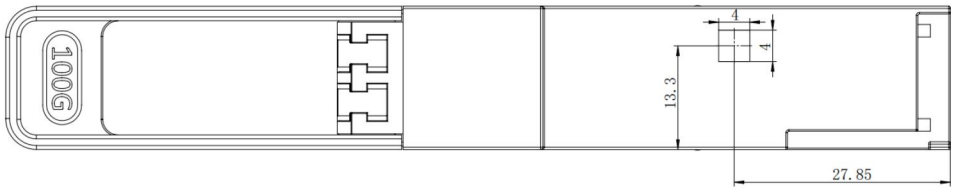

Figure 10: Case Temperature Measurement Point (Unit: mm)

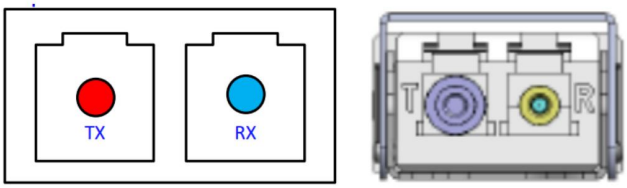

Figure 11: Module Optical Interface (looking into the optical port)

Ordering information

Part Number	Product Description
QFP-DWxxHG-80DC	100G QSFP28 DWDM, CH15~CH61, DWDM Wavelengths, Dual LC Connectors, 80km reach, with DDM, 0°C~+70°C

Wavelength Table

Ch. No.	Frequency (THz)	Center Wavelength(nm)	Ch. No.	Frequency (THz)	Center Wavelength(nm)
C15	191.50	1565.50	C16	191.60	1564.68
C17	191.70	1563.86	C18	191.80	1563.05
C19	191.90	1562.23	C20	192.00	1561.42
C21	192.10	1560.61	C22	192.20	1559.79
C23	192.30	1558.98	C24	192.40	1558.17
C25	192.50	1557.36	C26	192.60	1556.55
C27	192.70	1555.75	C28	192.80	1554.94
C29	192.90	1554.13	C30	193.00	1553.33
C31	193.10	1552.52	C32	193.20	1551.72
C33	193.30	1550.92	C34	193.40	1550.12
C35	193.50	1549.32	C36	193.60	1548.51
C37	193.70	1547.72	C38	193.80	1546.92
C39	193.90	1546.12	C40	194.00	1545.32
C41	194.10	1544.53	C42	194.20	1543.73
C43	194.30	1542.94	C44	194.40	1542.14
C45	194.50	1541.35	C46	194.60	1540.56
C47	194.70	1539.77	C48	194.80	1538.98
C49	194.90	1538.19	C50	195.00	1537.40
C51	195.10	1536.61	C52	195.20	1535.82
C53	195.30	1535.04	C54	195.40	1534.25
C55	195.50	1533.47	C56	195.60	1532.68
C57	195.70	1531.90	C58	195.80	1531.12
C59	195.90	1530.33	C60	196.00	1529.55
C61	196.10	1528.77			

For More Information

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